SONY

CXA3218N

FM Demodulator for BS/CS

Description

The CXA3218N is the video signal demodulation IC for satellite broadcasting. This IC has most of the functions required for demodulation, and provides stable video detection in combination with the CXA3108Q (L-band down converter with PLL).

Features

- Built-in IF AGC
- Excellent DG/DP characteristics
- Keyed AFT input pin to support MUSE reception
- 1st AGC control output pin
- Single 5 V power supply operation

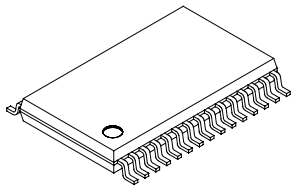
Applications

PAL/NTSC system BS tuners, etc.

Structure

Bipolar silicon monolithic IC

30P pin SSOP (Plastic)



Absolute Maximum Ratings (Ta=25 °C)

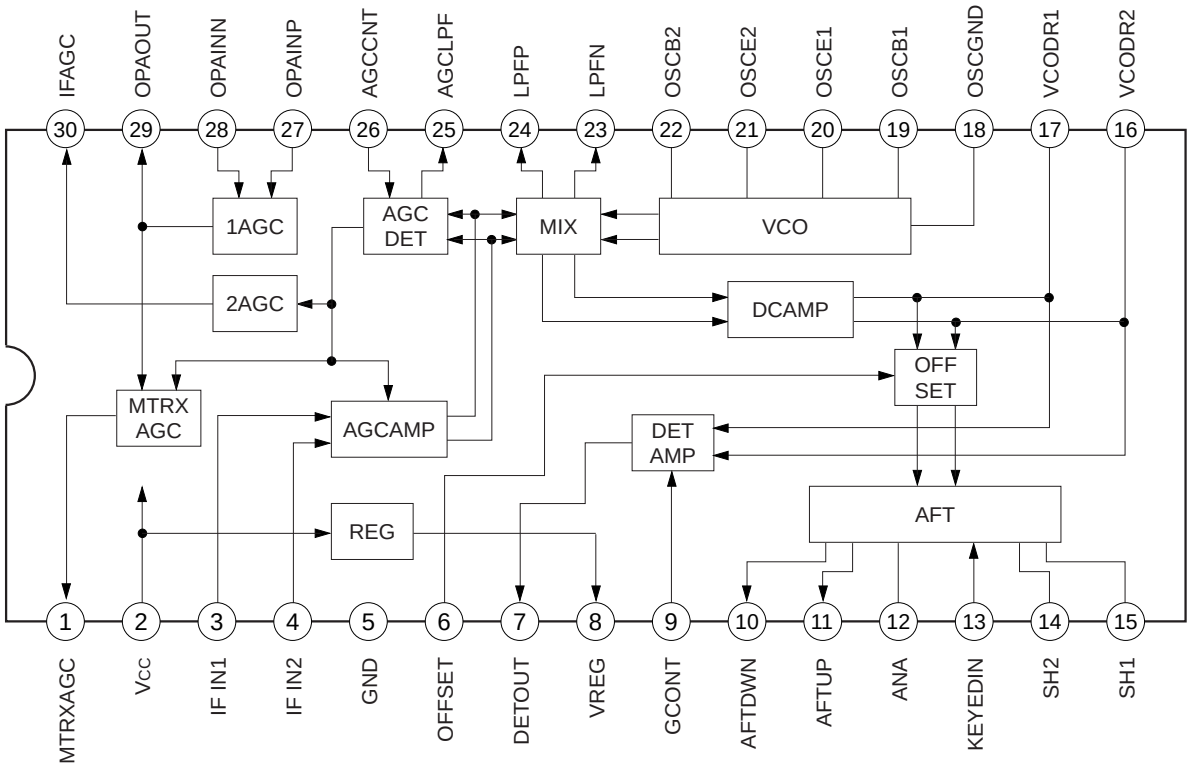
• Supply voltage	V_{CC}	–0.3 to 7.0	V
• Storage temperature	Tstg	–55 to +150	°C
• Allowable power dissipation	P_D	1000	mW

Operating Conditions

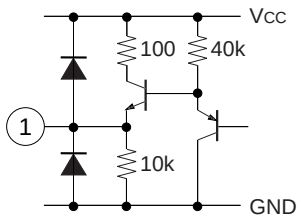
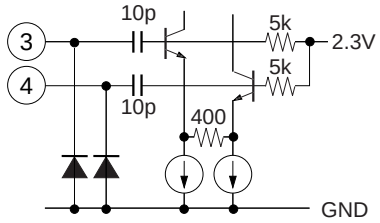
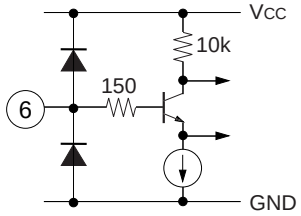
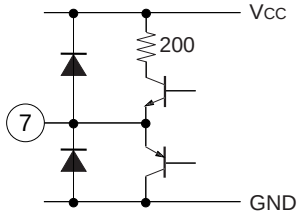
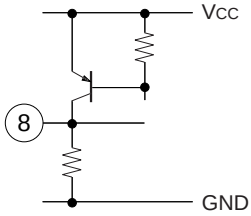
• Supply voltage	V_{CC}	4.50 to 5.50	V
• Operating temperature	Topr	–35 to +85	°C

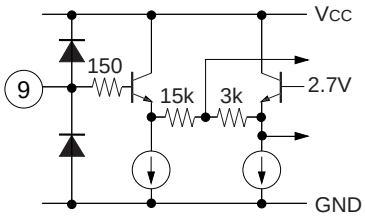
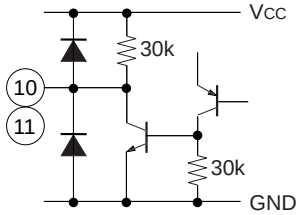
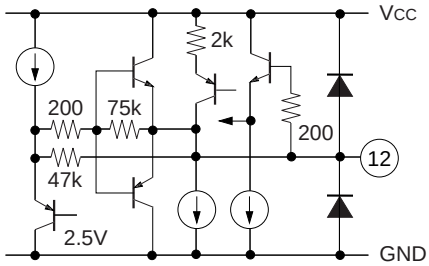
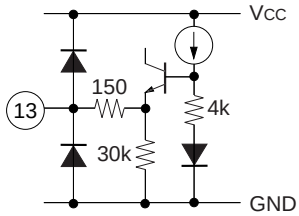
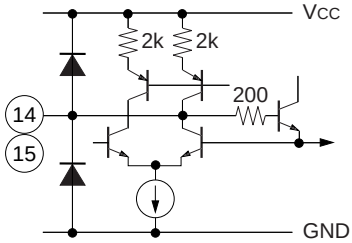
E98X25-TE

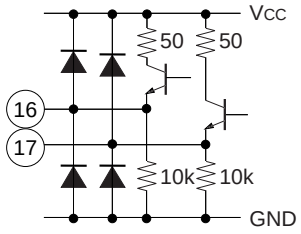
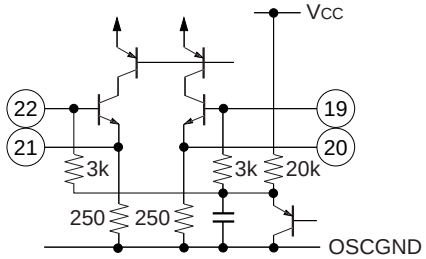
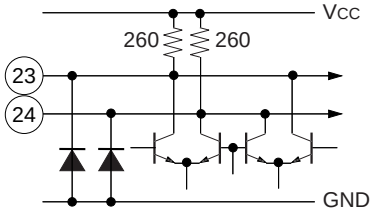
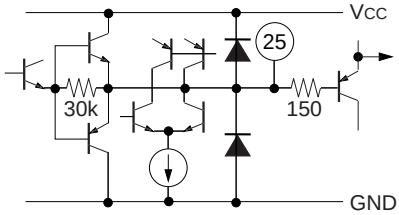
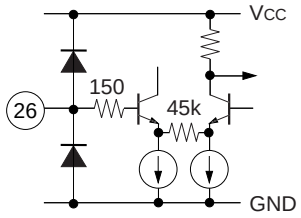
Block Diagram and Pin Configuration (Top View)

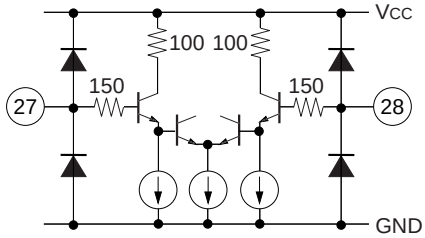
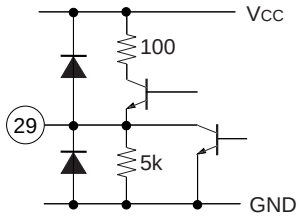
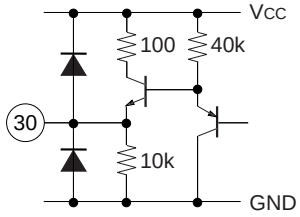


Pin Description

Pin No.	Symbol	Typical pin voltage	Equivalent circuit	Description
1	MTRXAGC	2.0 V to 3.5 V		AGC detection block MTRX-AGC analog output.
2	Vcc	5 V		Positive power supply.
3	IF IN1			AGC block IF input.
4	IF IN2			
5	GND	0 V		Ground.
6	OFFSET	2.0 V to 4.0 V		AFT block offset adjustment.
7	DETOUT	2.45 V		DETAMP block video output.
8	VREG	4.1 V		Reference voltage output. Connect to GND with a 10 µF capacitor.

Pin No.	Symbol	Typical pin voltage	Equivalent circuit	Description
9	GCONT	1.5 V to 4.0 V		DETAMP block gain adjustment.
10	AFTDWN	4.9 V or 0.1 V		AFT block digital output.
11	AFTUP			
12	ANA	2.4 V to 3.8 V		AFT block filter. Connect to GND with a 10 µF capacitor.
13	KEYEDIN	0.3 V		AFT block keyed input.
14	SH2	3.0 V to 3.5 V		AFT block sample-and-hold signal output. Connect to GND with a 0.1 µF capacitor.
15	SH1			

Pin No.	Symbol	Typical pin voltage	Equivalent circuit	Description
16	VCODR2	2.0 V to 3.0 V		PLL detection output.
17	VCODR1			
18	OSCGND	0 V		Ground.
19	OSCB1	1.4 V		VCO resonance circuit connect terminals.
20	OSCE1	0.7 V		
21	OSCE2	0.7 V		
22	OSCB2	1.4 V		
23	LPFN	4.5 V		PLL loop filter connect terminals.
24	LPFP			
25	AGCLPF	2.9 V to 3.0 V		AGC detection block filter. Connect to GND with a 0.01 µF capacitor.
26	AGCCNT	1.5 V to 3.5 V		AGC detection block gain adjustment.

Pin No.	Symbol	Typical pin voltage	Equivalent circuit	Description
27	OPAINP	1.5 V to 3.5 V		AGC detection block 1st AGC input.
28	OPAINN			
29	OPAOUT	0.3 V or 3.5 V		AGC detection block 1st digital output.
30	IFAGC	2.0 V to 3.0 V		AGC detection block 2nd analog output.

Electrical Characteristics

DC Characteristics

(Ta=25 °C, V_{CC}=5 V, See the Electrical Characteristics Measurement Circuit.)

	Item	Pin	Symbol	Conditions	Min.	Typ.	Max.	Unit
1	Current consumption	2	I_{CC}	When no signal input	65	80	95	mA
2-1	AGC-1 High output voltage	29	VAGC1H	Vin=–60 dBm, Pin 26=3.0 V, Pin 27=2.5 V	3.0	3.5	3.7	V
2-2	AGC-1 Low output voltage	29	VAGC1L	Vin=–10 dBm Pin 26=3.0 V, Pin 27=2.5 V	0.1	0.3	1.0	
3-1	AGC-2 High output voltage	30	VAGC2H	Vin=–10 dBm, Pin 26=3.0 V	2.6	2.9	3.2	
3-2	AGC-2 Low output voltage	30	VAGC2L	Vin=–60 dBm, Pin 26=3.0 V	1.5	2	2.4	
4-1	AGC-MTRX High output voltage	1	VMTRH	Vin=–10 dBm, Pin 26=3.0 V, Pin 27=2.5 V	3.0	3.5	3.7	
4-2	AGC-MTRX Low output voltage	1	VMTRL	Vin=–60 dBm, Pin 26=3.0 V, Pin 27=2.5 V	1.5	2.3	2.7	
5	VCODR 1/2 output voltage	16, 17	VVCD	400 MHz input	2.0	2.5	3.0	
6	VCODR 1/2 driver current capacitance	16, 17	IVCD	Load resistance RL=1 kΩ	2.0	2.5	3	mA
7	VREG output voltage	8	VREG		3.9	4.15	4.4	V
8	SH 1/2 leak current	14, 15	ISH	KEYEDIN=0.5 V	0	0.3	0.7	µA

AC Characteristics (AGC)

(Ta=25 °C, V_{CC}=5 V, See the Electrical Characteristics Measurement Circuit.)

	Item	Pin	Symbol	Conditions	Min.	Typ.	Max.	Unit
11	IF input frequency	3, 4	fin		—	400	—	MHz
12	IF input level	3, 4	Vin	One amplitude for balance input	–60	—	–10	dBm
13	1st AGC change point (input level)	29	AGC1	Pin 26=2.5 V, Pin 27=2.5 V	—	–45	—	
14	1st AGC control sensitivity	29	Δ AGC	Slope of variation	—	–0.8	—	V/dB
15	1st AGC adjustment sensitivity	29	AGC1/V	Variation of change point/ Pin 27 DC variation	—	42	—	dB/V
16	2nd AGC control sensitivity	30	Δ AGC2	Slope of variation	18	24	30	mV/dB
17	2nd AGC adjustment sensitivity	30	AGC2/V	Variation of change point/ Pin 26 DC variation	3	11	18	dB/V
18	AGC-MTRX control sensitivity	1	Δ MTRX	Slope of variation	—	0.3	—	V/dB

AGC Characteristics (PLL) (Ta=25 °C, V_{CC}=5 V, See the Electrical Characteristics Measurement Circuit.)

	Item	Pin	Symbol	Conditions	Min.	Typ.	Max.	Unit
21	VCO variation sensitivity		β	*1	32	37	42	MHz/V
22	VCO oscillation frequency		fosc	*1	—	400	—	MHz
23	PLL capture range		CAP	Sum of positive/negative polarities *1	—	40	—	
24	DETOUT level	7	VOUT	Dev.=17 MHzpp, Pin 9=2.7 V	0.60	0.68	0.76	Vp-p
25-1	DETOUT level variable range 1	7	VPdB	VOUT=0 dB, Pin 9=+0.5 V	1	2	—	dB
25-2	DETOUT level variable range 2	7	VMdB	VOUT=0 dB, Pin 9=–0.5 V	—	–2	–1	dB
26	GCONT adjustment sensitivity	7	Δ VOUT	Output level/Pin 9 DC variation	2	4	6	dB/V
27	DETOUT frequency response (8 MHz)	7	VOUTf	8 MHz/1 MHz	–1	0	1	dB

*1 Varies according to the external constant (coil, varicap).
This characteristic is for NTSC, and it works at 480 MHz for PAL.

AC Characteristics (Video) (Ta=25 °C, V_{CC}=5 V, See the Electrical Characteristics Measurement Circuit.)

	Item	Pin	Symbol	Conditions	Min.	Typ.	Max.	Unit
31	IF → DET output DG	7	DGA	IF input *1	0	0.3	1.5	%
32	IF → DET output DP	7	DPA	IF input *1	–2	0	2	deg
33	fsc beat suppression level	7	IMA	IF input	40	45	—	dB
34	IF → DET output S/N	7	CSN	IF input	55	60	—	dB

*1 Varies according to the external constant (coil, varicap).

AC characteristics (AFT) (Ta=25 °C, V_{CC}=5 V, See the Electrical Characteristics Measurement Circuit.)

	Item	Pin	Symbol	Conditions	Min.	Typ.	Max.	Unit
42	AFT offset adjustment sensitivity	6	fAFT/V	f0 variation/Pin 6 DC variation	5	8	12	MHz/V
43	AFT dead zone width		fAFT/D		60	180	360	kHz
44	AFTUP/AFTDOWN Low	10, 11	AFTL		0	0.1	0.4	V
45	AFTUP/AFTDOWN High	10, 11	AFTH		4.7	4.9	V_{CC}	

Description of Operation

The CXA3218N consists of the following four function blocks. First, the signal flow is explained briefly, followed by the functions of each block.

(1) AGC circuit
(2) FM demodulation circuit
(3) Detection signal amplification circuit
(4) AFT circuit

The 2nd IF differential signal input to IF IN1 and IF IN2 (Pins 3 and 4) passes through the AGC circuit to fix the signal level and is then input to the FM demodulation circuit.
The FM demodulated signal by the PLL demodulation circuit is then input to the DETAMP circuit and AFT circuit.
The AFT circuit detects the frequency error of the 2nd IF signal by the detection output voltage value, and outputs a command to the external frequency conversion circuits in order to correct the local frequency.

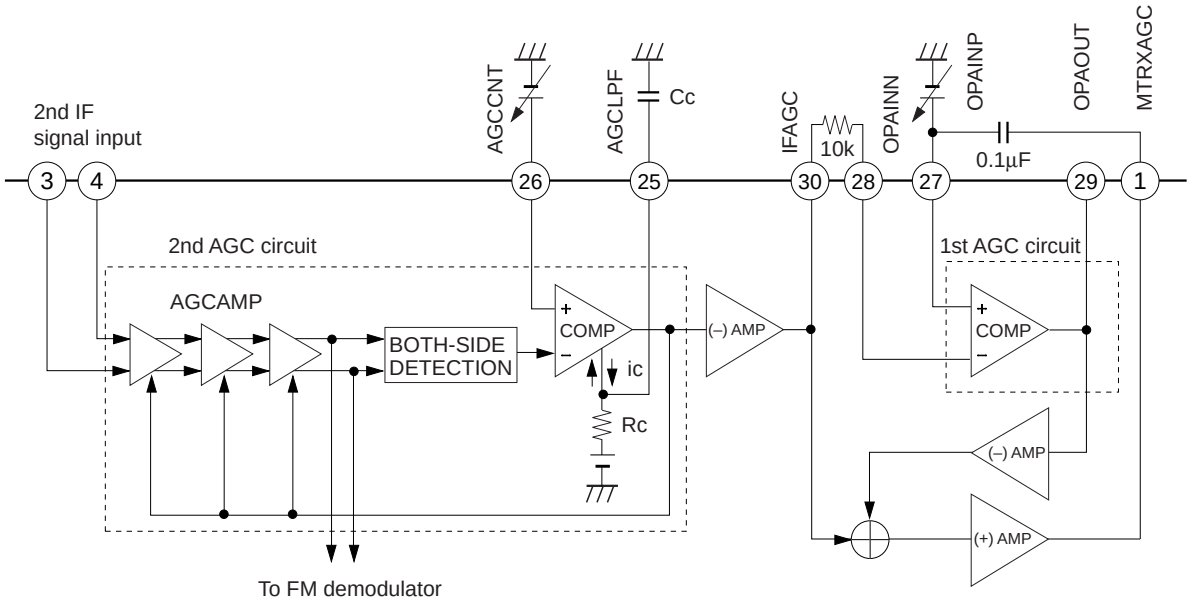
(1) AGC circuit

The 2nd IF differential signal is input to IF IN1 and IF IN2 (Pins 3 and 4) to fix the signal level by the AGC circuit. A capacitor which determines the AGC loop time constant is connected to AGCLPF (Pin 25), and the adjustment voltage at the AGC (2nd AGC) output setting level is applied to AGCCNT (Pin 26).

The 2nd AGC control voltage is output from IFAGC (Pin 30). The 1st AGC starting level adjustment voltage for the 1st IF is applied to OPAINP (Pin 27). The MTRXAGC (Pin 1) output is input through a 0.1 µF capacitor.

The IFAGC (Pin 30) output is input to OPAINN (Pin 28) through a 10 kΩ resistor, and the 1st AGC control voltage is output from OPAOUT (Pin 29). At this time, the IFAGC (Pin 30) output is used at the linear portion against the input level. (See the Example of Representative Characteristics.)

The add voltage of the negative characteristics of the OPAOUT (Pin 29) output 1st AGC control voltage and the IFAGC (Pin 30) output 2nd AGC control voltage is output from MTRXAGC (Pin 1).



(2) FM demodulation circuit

The FM demodulation circuit is a PLL demodulator which consists of an oscillator (OSC.), phase discriminator and DCAMP. The oscillator resonance circuit is connected to OSCB1 to OSCB2 (Pins 19 to 22) and the loop filter to LPFN (Pin 23) and LPFP (Pin 24). The DCAMP differential output comes from VCODR2 (Pin 16) and VCODR1 (Pin 17), and this output is used as the drive voltage for the varicap that comprises the oscillator.

(3) Detection signal amplification circuit

The signal which is detected by the FM demodulation circuit is amplified at DETAMP circuit and then output from DETOUT (Pin 7). The gain of this amplification circuit can be adjusted by the voltage applied to GCONT (Pin 9).

(4) AFT circuit

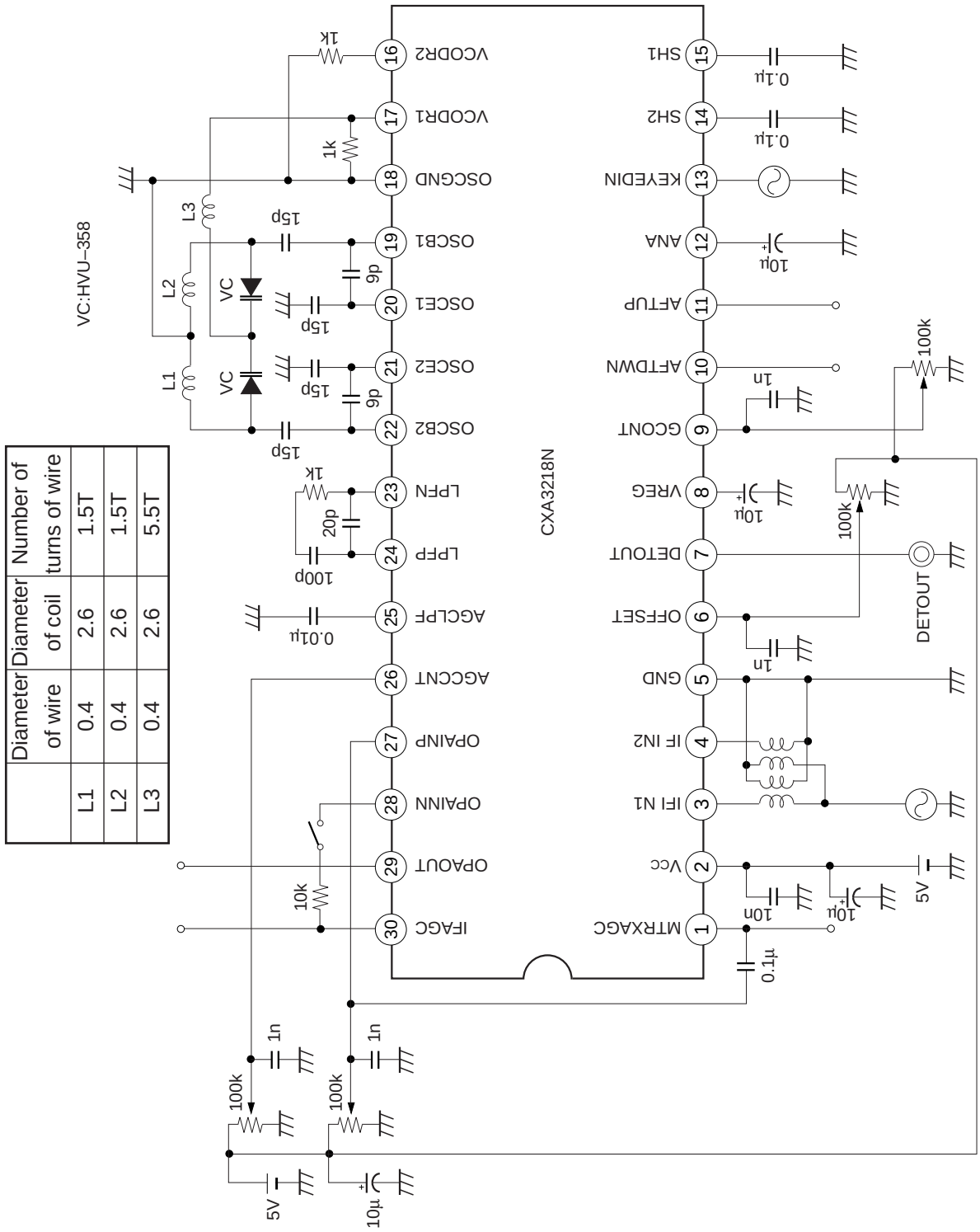
The AFT circuit detects the frequency error in the 2nd IF signal as a voltage displacement from the FM demodulation signal input to the AFT block, and outputs the two values of High (5 V) or Low (0 V) from AFTDWN (Pin 10) and AFTUP (Pin 11). High indicates the frequency change command (active-High). Furthermore, the High output from both pins indicates the dead zone. The LPF capacitor is connected to ANA (Pin 12) and the keyed pulse for the keyed AFT is input to KEYEDIN (Pin 13). The KEYEDIN (Pin 13) voltage should be 0 V during mean AFT value. The sample-and-hold capacitors are connected to SH2 (Pin 14) and SH1 (Pin 15).

Apply the offset adjustment voltage to OFFSET (Pin 6) to cancel the effects of the DC offset in the IC.

(5) Other

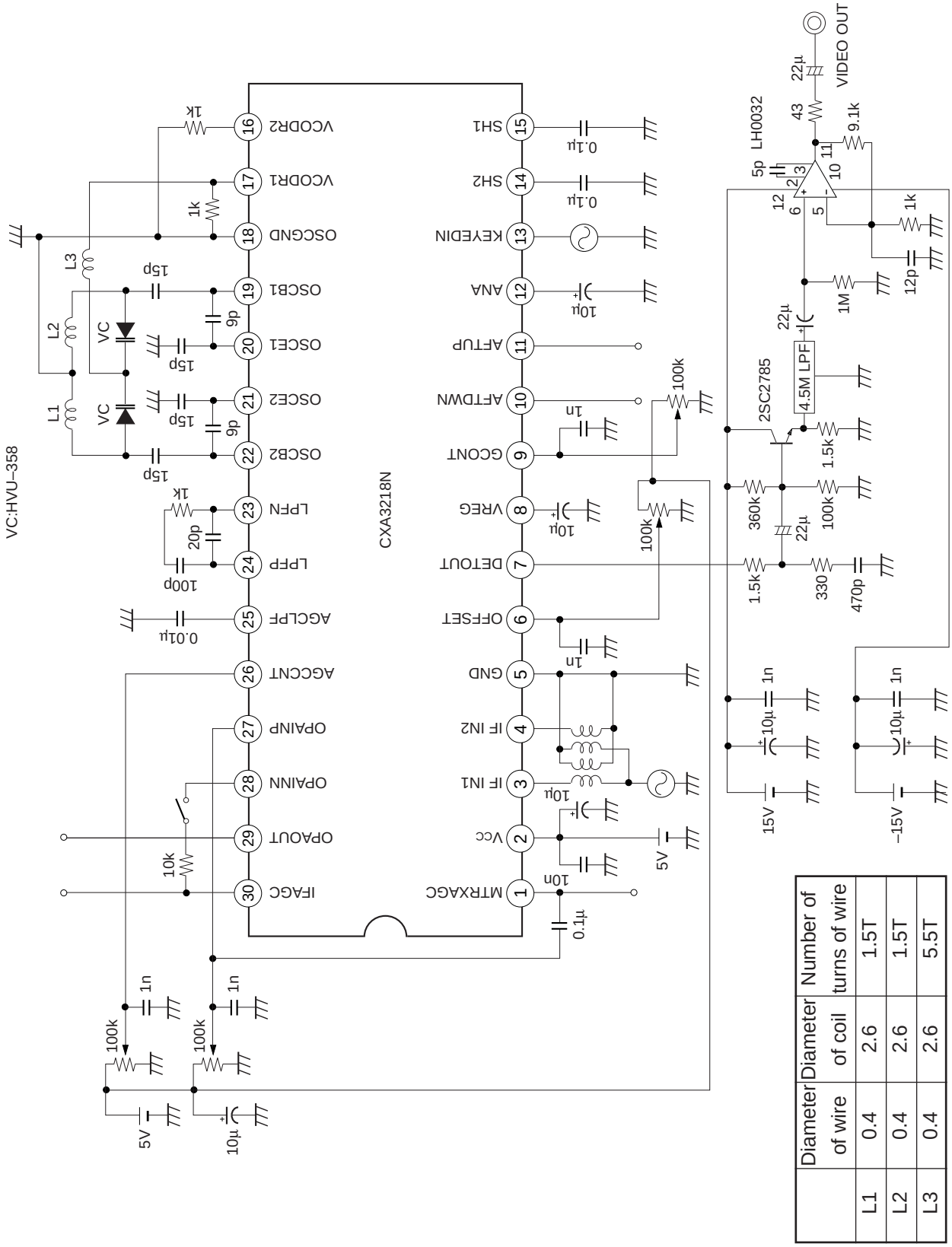
A capacitor is connected to eliminate the regulator voltage noise to VREG (Pin 8), and use this output as the reference voltage for internal adjustment.

Electrical Characteristics Measurement Circuit 1



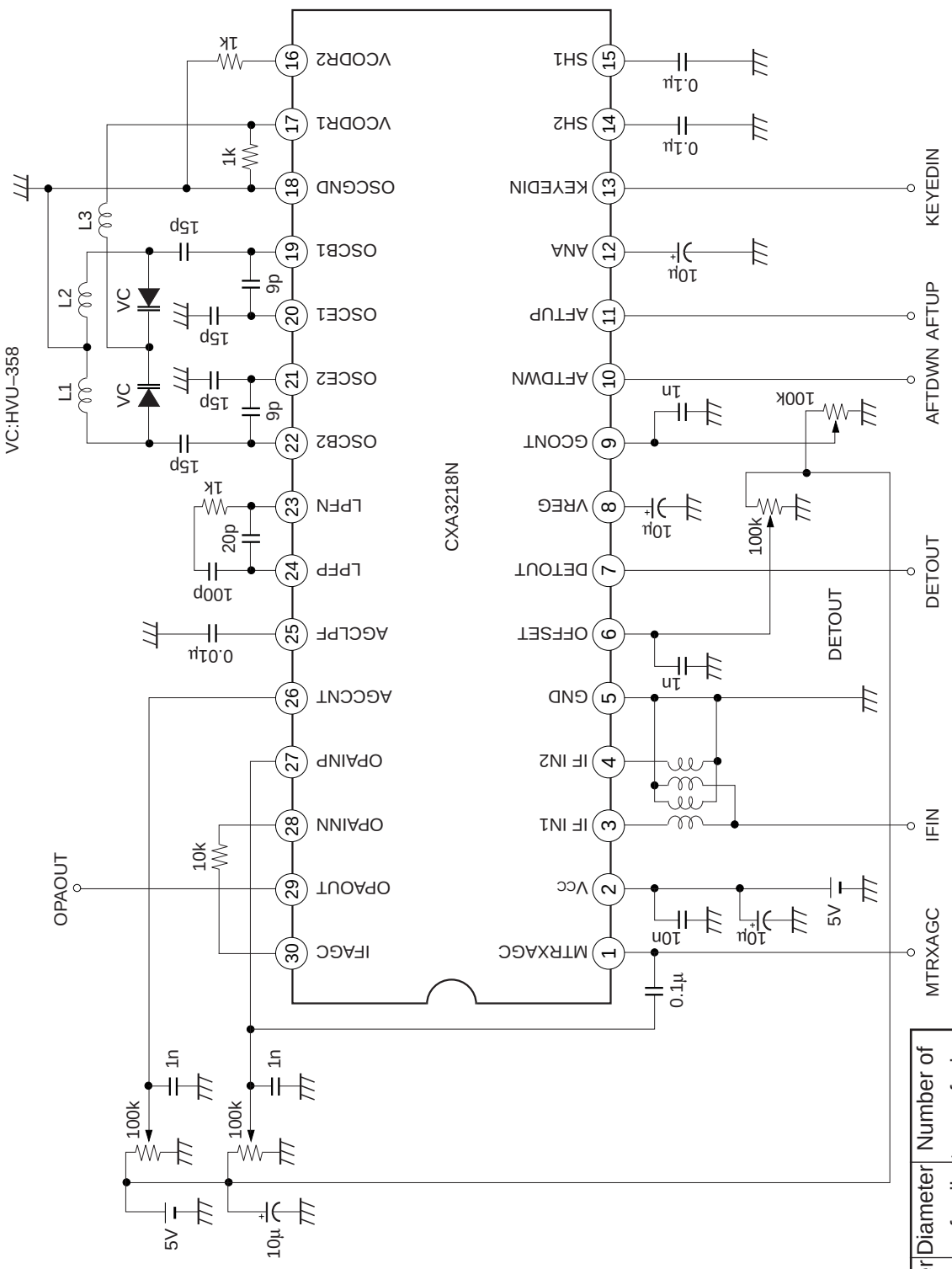
	Diameter of wire	Diameter of coil	Number of turns of wire
L1	0.4	2.6	1.5T
L2	0.4	2.6	1.5T
L3	0.4	2.6	5.5T

Electrical Characteristics Measurement Circuit 2



	Diameter of wire	Diameter of coil	Number of turns of wire
L1	0.4	2.6	1.5T
L2	0.4	2.6	1.5T
L3	0.4	2.6	5.5T

Application Circuit

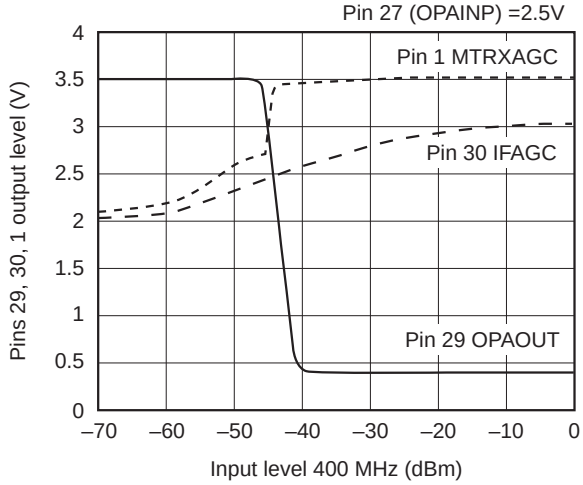


	Diameter of wire	Diameter of coil	Number of turns of wire
L1	0.4	2.6	1.5T
L2	0.4	2.6	1.5T
L3	0.4	2.6	5.5T

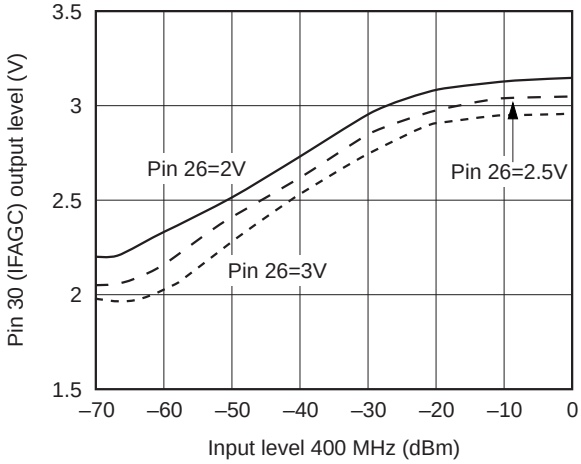
Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

Example of Representative Characteristics

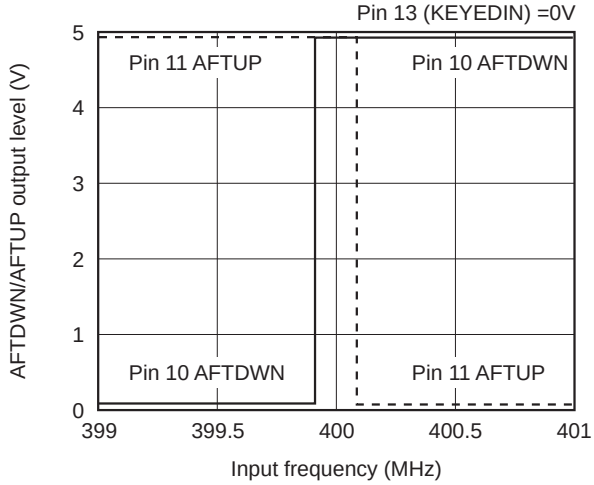
AGCDET characteristics
Pin 26 (AGCCNT) =2.5V
Pin 27 (OPAINP) =2.5V



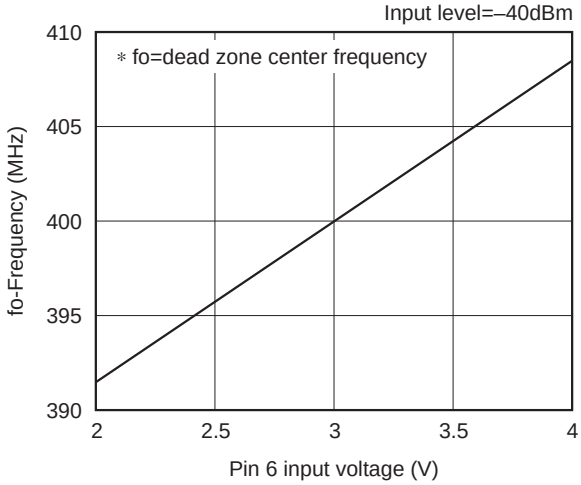
IFAGC characteristics



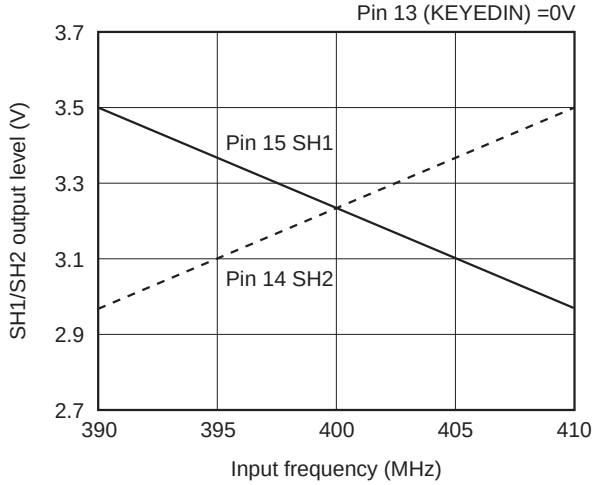
AFT characteristics
Pin 6 (OFFSET) =3V
Pin 13 (KEYEDIN) =0V



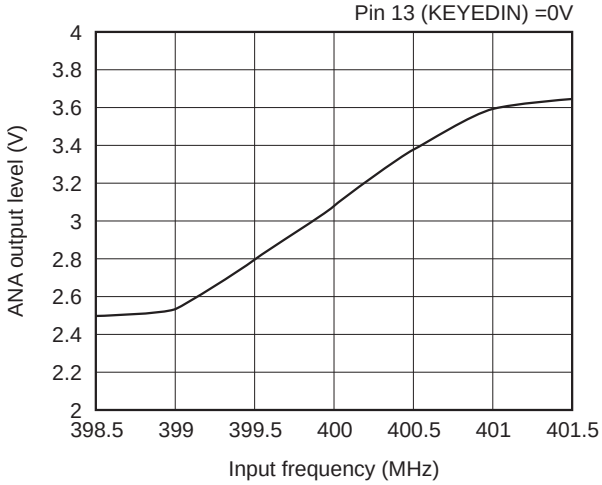
AFT offset adjustment sensitivity characteristics
Input level=–40dBm



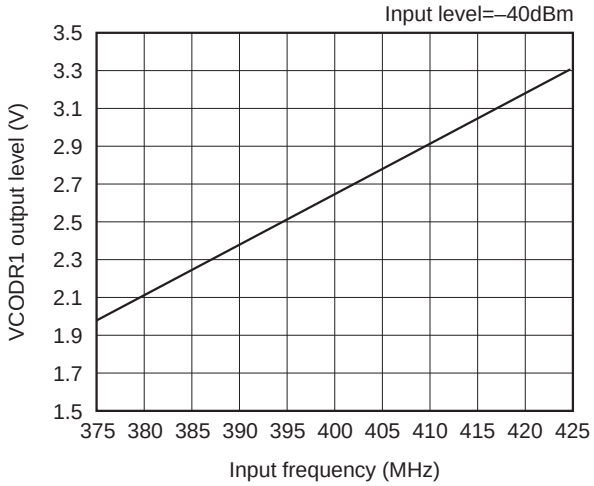
SH pin voltage characteristics
Pin 6 (OFFSET) =3V
Pin 13 (KEYEDIN) =0V



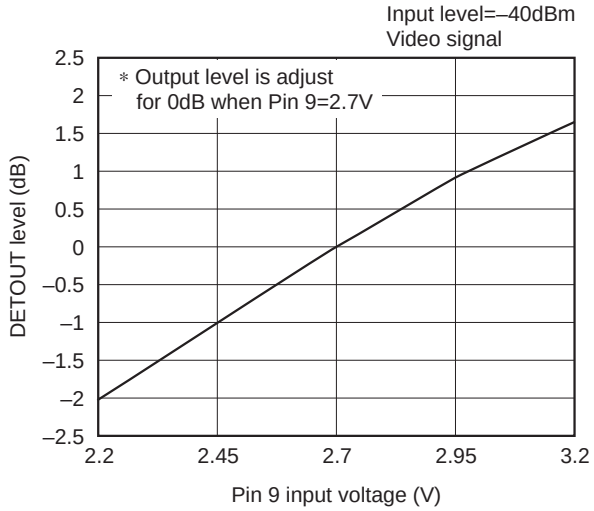
ANA pin voltage characteristics
Pin 6 (OFFSET) =3V
Pin 13 (KEYEDIN) =0V



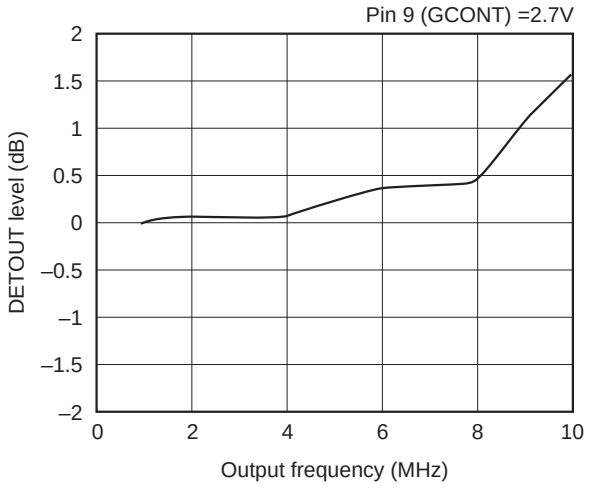
PLL lock characteristics



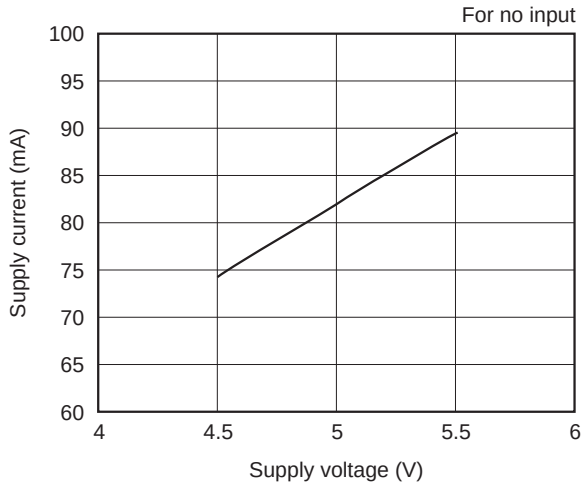
GCONT adjustment sensitivity



DETOUT characteristics

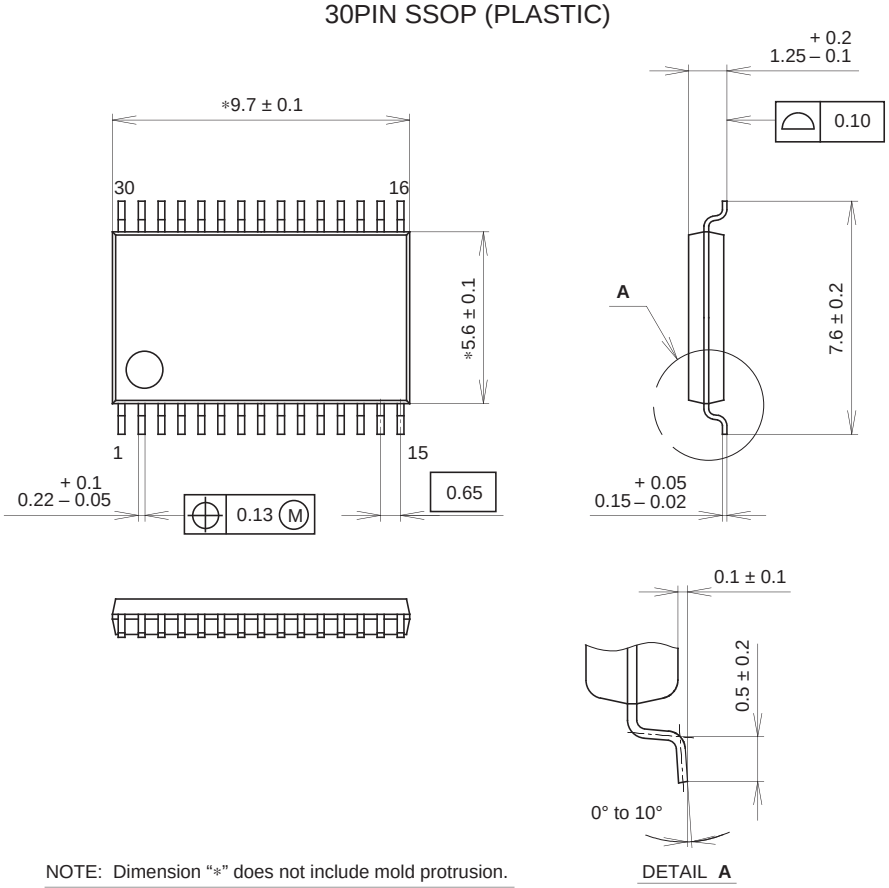


Supply current vs. Supply voltage



Package Outline Unit : mm

30PIN SSOP (PLASTIC)



NOTE: Dimension "∗" does not include mold protrusion.

DETAIL **A**

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER/PALLADIUM PLATING
LEAD MATERIAL	42/COPPER ALLOY
PACKAGE MASS	0.1g

SONY CODE	SSOP-30P-L01
EIAJ CODE	SSOP030-P-0056
JEDEC CODE	————

NOTE : PALLADIUM PLATING
This product uses S-PdPPF (Sony Spec.-Palladium Pre-Plated Lead Frame).